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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,709	04/04/2001	Hideki Kabune	1-129	1768

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EXAMINER	
YANCHUS III, PAUL B	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/824,709	Applicant(s) KABUNE ET AL.	
	Examiner Paul B Yanchus	Art Unit 2116	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6 and 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This final office action is in response to communications filed on 11/16/04.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al., US Patent no. 5,339,446, in view of Curinger et al., US Patent no. 6,330,668.

Regarding claims 1 and 6, Yamasaki et al. teaches an electronic control apparatus comprising:

a plurality of power source circuits [POWER OUTPUT in Figure 1] providing a plurality of power sources of a plurality of different voltages [outputs of power supply section, column 3, lines 5-10]; and

a microcomputer [COMPUTER SYSTEM in Figure 1], wherein any one of the plurality of power sources is used as a power source of the microcomputer [POWER OUTPUT in Figure 1 and column 3, lines 60-67].

Yamasaki et al. also teaches detecting if any one of the plurality of power sources is not set to a voltage in respective specified ranges by checking whether the plurality of power sources are respectively set to the voltages in the specified ranges [column 3, lines 17-25].

Yamasaki et al. teaches stopping the power supply when it is detected that any of the power sources output a voltage that is outside of a normal range [column 3, lines 17-25], but does not explicitly teach resetting the microcomputer when a voltage abnormality is detected. Curinger et al. discloses resetting a microcontroller immediately after it is detected that the voltage supply drops below a predetermined voltage [column 6, lines 43-56].

It would have been obvious to one of ordinary skill in the art to incorporate the teachings of Curinger et al. into the Yamasaki et al. apparatus. Resetting a microcomputer immediately after it is detected that a power source output is not in the proper voltage range ensures that the microcomputer will not perform incorrect calculations [column 1, lines 64-67 and column 2, lines 12-17].

Regarding claim 2, Yamasaki et al. teaches that the power source circuits have a first power output circuit outputting a first voltage [+12 V] that is applied to a peripheral circuit [RS232C port, column 3, lines 45-67], and a second power output circuit outputting a second voltage [+5 V] that is lower than the first voltage and applied to the reset control unit, the oscillation circuit and the CPU [computer system, column 3, lines 45-67]. Yamasaki et al. does not explicitly show an analog-digital converting unit, a reset control circuit and an oscillation circuit, but it is well known in the art that conventional computer systems have an analog-digital converting unit, a reset control unit to reset the CPU and an oscillation circuit to provide a clocking signal to the CPU.

Yamasaki et al. and Curinger et al., as described above, teach detecting if any one of the plurality of power sources is not set to a voltage in respective specified ranges and resetting the

microcomputer if one of the power sources is not set to a voltage in the respective specified ranges.

Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al., US Patent no. 5,339,446 and Curinger et al., US Patent no. 6,330,668, in view of Carter, US Patent no. 6,298,449.

Regarding claim 3, Yamasaki et al. and Curinger et al., as described above, teach detecting if any one of the plurality of power sources is not set to a voltage in respective specified ranges and resetting the microcomputer if one of the power sources is not set to a voltage in the respective specified ranges. Yamasaki et al. and Curinger et al. do not explicitly teach detecting if any of the plurality of power sources is not set to a current in respective specified ranges. Carter teaches detecting if current being input to a computer deviates from a predetermined range [column 5, lines 20-43, column 6, lines 8-23 and column 9, lines 14-16].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Yamasaki et al. and Nakajima with the teachings of Carter. According to Carter, abnormal current levels can be a strong indication of a computer failure [column 5, lines 25-27]. Detecting abnormal current levels in addition to abnormal voltage levels in a computer system provides an extra level of fault detection to which leads to improved system reliability.

Regarding claim 7, Yamasaki et al. teaches an electronic control apparatus comprising:

first and second power source circuits [POWER OUTPUT in Figure 1] providing first and second power sources with first and second voltages different from one another, respectively [outputs of power supply section, column 3, lines 5-10];

a microcomputer [COMPUTER SYSTEM in Figure 1] connected to the first and second power source circuits and operable with the first and second voltages [POWER OUTPUT in Figure 1 and column 3, lines 60-67];

a first abnormality detection circuit for detecting an abnormal value of the first voltage and an abnormal value of a first current in the first power source circuit, the abnormal levels of the first voltage and the first current being outside predetermined first voltage range [column 3, lines 17-25];

a second abnormality detection circuit for detecting an abnormal value of the second voltage and an abnormal value of a second current in the second power source circuit, the abnormal values of the second voltage and the second current being outside predetermined second voltage range [column 3, lines 17-25]; and

Yamasaki et al. teaches stopping the power supply when it is detected that any of the power sources output a voltage that is outside of a normal range [column 3, lines 17-25], but does not explicitly teach resetting the microcomputer when a voltage abnormality is detected. Curinger et al. discloses resetting a microcontroller immediately after it is detected that the voltage supply drops below a predetermined voltage [column 6, lines 43-56].

It would have been obvious to one of ordinary skill in the art to incorporate the teachings of Curinger et al. into the Yamasaki et al. apparatus. Resetting a microcomputer immediately after it is detected that a power source output is not in the proper voltage range ensures that the microcomputer will not perform incorrect calculations [column 1, lines 64-67 and column 2, lines 12-17].

Regarding claim 3, Yamasaki et al. and Curinger et al., as described above, teach detecting if any one of the plurality of power sources is not set to a voltage in respective specified ranges and resetting the microcomputer if one of the power sources is not set to a voltage in the respective specified ranges. Yamasaki et al. and Curinger et al. do not explicitly teach detecting if any of the plurality of power sources is not set to a current in respective specified ranges. Carter teaches detecting if current being input to a computer deviates from a predetermined range [column 5, lines 20-43, column 6, lines 8-23 and column 9, lines 14-16].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Yamasaki et al. and Nakajima with the teachings of Carter. According to Carter, abnormal current levels can be a strong indication of a computer failure [column 5, lines 25-27]. Detecting abnormal current levels in addition to abnormal voltage levels in a computer system provides an extra level of fault detection to which leads to improved system reliability.

Response to Arguments

Applicant's arguments with respect to claims 1-3 and 6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
December 8, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER ~~3600~~ 2100